IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Barnett	Docket No:	TI-36636
Serial No:	10/805,928	Examiner:	Negron, Daniell
Filed:	3/22/2004	Art Unit:	2651
For:	WRITE CURRENT WAVEFORM ASYMMETRY COMPENSATION		

APPEAL BRIEF PURSUANT TO 1.192(c)

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at **571-273-8300** on March 21, 2006:

Tommie Chambers

Tommie Chambers

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in connection with the above identified application in response to the final Office Action mailed September 7, 2005.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

RECEIVED
CENTRAL FAX CENTER

MAR 2 1 2006

STATUS OF THE CLAIMS

Claims 1-19 were originally filed, and no claims have been added or cancelled.

Consequently the subject matter of the instant appeal is the final rejection of Claims 1-19.

STATUS OF AMENDMENTS

The application was originally filed with Claims 1-19.

A response after final was filed on December 1, 2005 amending some of the claims.

There was no Advisory Action; consequently, Applicants assume that the response has been entered.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Referring now to Figure 2A there is illustrated a simplified H-bridge type circuit typically used for driving current through a write head 202 in a hard disk drive system. The purpose of the H-bridge is to enable current to be driven through the write head in either direction in which the H-bridge includes both a positive 204 and negative 206 side as is known in the art. The simplified circuit also includes an write current overshoot amplitude DAC 212 coupled to the conventional write driver circuitry 208, 210 for controlling the write current overshoot amplitude equally for each of the positive 204 and negative 206 portions of the H-bridge. Also included is a write current overshoot duration DAC 214 coupled to the conventional write driver circuitry 208, 210 for controlling the write current overshoot duration equally for each of the positive 204 and negative 206 portions of the H-bridge. Referring now to Figure 2B there is shown the write current overshoot amplitude pulsing signals, seen at node X and Node Y on

PAGE 4/14 * RCVD AT 3/21/2006 4:05:04 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-5/17 * DNIS:2738300 * CSID:972 917 4417 * DURATION (mm-ss):04-08

Figure 2A, typically used with the circuit shown in Figure 2A to equally generate the positive and negative write current overshoots amplitudes. As shown and described above, separate signals 211 and 221 are used to generate the positive edge and the negative edge write current overshoot amplitude. Conventionally, the amplitudes of the signals are designed to be equal in order to create a nice symmetrical write current overshoot amplitude.

Referring now to Figure 2C there is shown positive edge and negative edge write current overshoot duration control signals that are internal signals to block 208 and 210 on Figure 2A, used to equally generate the positive and negative write current overshoot durations. As shown and described above, separate signals 243 and 245 are equally delayed versions of the reference signal 241 and used to generate the positive edge and the negative edge write current overshoot duration. Conventionally, the delay of the duration control signals are designed to be equal in order to create a nice symmetrical write current overshoot durations.

An exemplary embodiment of the present invention comprises an individually positive edge and negative edge adjustable write current overshoot amplitude which enables a user to program out or adjust for system introduced asymmetries in the amplitude of the write current overshoot waveform. And, a further embodiment includes an individually positive and negative edge adjustable duration circuit enabling write current overshoot duration asymmetry adjustments which further improves overall system performance.

Referring now to Figure 3A there is shown a drive circuit 300 with an individual programmable positive and negative write current overshoot amplitude correction DAC 311 in accordance with exemplary embodiments of the present invention. Further, components of the circuit 300 include items 202, 204, 206, 208, 210, 212 and 214 which are the same as those shown in Figure 2A. The addition of the individually programmable positive and negative amplitude correction DAC 311 enables the resultant positive edge and negative edge write current overshoot amplitude signals to be individually compensated for. That is, block 311 enables selective programming of

the write current overshoot amplitude providing separate tuning for the positive and negative peak write current overshoot amplitude value.

Referring now to Figure 3B there is shown the write current overshoot amplitude pulsing signals, seen at node X and Node Y on Figure 3A, used with the circuit shown in Figure 3A to individually adjust the positive and negative write current overshoots amplitudes. As shown and described above, separate signals 331 and 333 are used to generate the positive edge and the negative edge write current overshoot amplitude. As shown on Figure 3B, the write current amplitude pulsing signals are no longer equal in amplitude thus purposefully introducing a non-symmetrical write current overshoot amplitude allowing the user to compensate for system induced write current overshoot asymmetries, for example.

Figure 3C illustrates a simulated write current having a waveform 341 with a +6mA asymmetry on the positive edge write current overshoot and a resultant waveform 343 in which the positive edge amplitude of the positive write current overshoot signal has been adjusted via the individual programmable positive and negative amplitude correction DAC 311 of the present invention until the asymmetry was removed. Range for individual amplitude programmability is determined by the system requirements but typically +/- 20% of the programmed equal amplitude is enough to compensate for system induced asymmetries.

Referring now to Figure 4A there is shown another exemplary embodiment including the addition of an individual programmable positive and negative write current overshoot duration correction DAC 411. Further, components of the circuit 400 include items 202, 204, 206, 208, 210, 212, 214 and 311 which are the same as those shown in Figure 3A. The addition of the individually programmable positive and negative duration correction DAC 411 is added to enable the resultant positive edge and negative edge write current overshoot duration signals to be individually compensated for. That is, block 411 enables selective programming of the write current overshoot duration providing separate tuning for the positive and negative peak write current overshoot duration value. This enables a user to not only selectively program the amplitude separately for each of the positive and negative amplitudes of the write

current overshoot signal but also selectively program the duration separately for each of the positive and negative durations of the write current overshoot signal.

Referring now to Figure 4B there is shown positive edge and negative edge write current overshoot duration control signals that are internal signals to block 208 and 210 on Figure 4A, used to generate the positive and negative write current overshoot durations. As shown and described above, separate signals 433 and 435 are individually delayed versions of the reference signal 431 and used to generate the positive edge and the negative edge write current overshoot duration. As shown on Figure 4B, the write current duration control signals are no longer equal in amplitude thus purposefully introducing a non-symmetrical write current overshoot duration allowing the user to compensate for system induced write current overshoot duration asymmetries, for example.

Figure 4C illustrates a simulated write current having a waveform 441 with a 45pS write current overshoot duration asymmetry and a resultant waveform 443 in which the duration of the positive write current overshoot signal has been adjusted via the individual duration control circuit 411 of the present invention until the asymmetry was removed. Range for individual duration programmability is determined by the system requirements but typically +/- 20% of the equally programmed duration is enough to compensate for system induced asymmetries.

To summarize, a system and/or method is provided for correcting the inherent imbalance associated with the read/write head interconnects which cause unbalanced loading on the differential write data path in which this unbalanced loading induces an asymmetry in the write current overshoot signal amplitude and duration. An asymmetrical write current introduces unwanted jitter into the write data and ultimately degrades the bit error rate of the signal. The write driver overshoot current signal is programmed to counter-act system induced imbalances in the write signal.

GROUNDS OF REJECTION

The sole ground on rejection is whether or not Claims 1-19 are anticipated by Lacombe.

ARGUMENTS

It is respectfully submitted that Lacombe does not disclose or suggest the presently claimed invention including the circuit coupled to the write head driver circuit and adaptive to selectively provide pulsing signals which define independently an overshoot amplitude of the positive write edge and the negative write edge respective of the write current signal.

Lacombe discloses at column 9, lines 20-25 that signals WBX and WBY will not toggle immediately but will be delayed by a delay circuit, and the delay period determines the duration of the coil overshoot current.

Consequently, WBX and WBY do not relate to the amplitude but relate to the duration of the coil overshoot current. There is no independent control of the positive and negative write edge.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-19 under 35 U.S.C. § 102 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

W. Daniel Swayze, Jr.
Attorney for Appellants
Reg. No. 34,478

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-5633

APPENDIX

Claim 1 (previously presented): A write current circuit for a mass media write head, comprising:

a head write driver circuit adapted to drive the write head with a write current signal having a positive write edge and a negative write edge; and

a circuit coupled with the head write driver circuit and adapted to selectively provide pulsing signals which independently define an overshoot amplitude of said positive write edge and said negative write edge respectively of said write current signal.

Claim 2 (original): The write current circuit of Claim 1, wherein said further circuit is a differential current source.

Claim 3 (original): The write current circuit of Claim 2, wherein said differential current source is programmable.

Claim 4 (previously presented): The write current circuit of Claim 1, wherein said further circuit is adapted to selectively provide a defined amplitude.

Claim 5 (original): The write current circuit of Claim 4, wherein said further circuit is programmable for providing differential overshoot amplitudes for said positive write edge and said negative write edge.

Claim 6 (original): The write current circuit of Claim 1, wherein said further circuit includes a delay circuit for selectively providing a defined pulse width for each of said overshoots.

Claim 7 (original): The write current circuit of Claim 6, wherein said delay circuit is programmable for providing differential overshoot pulse widths for said positive write edge and said negative write edge.

Claim 8 (original): The write current circuit of Claim 1, wherein said further circuit is adapted to selectively provide a defined amplitude of each of said overshoots and includes a delay circuit for providing a defined pulse width for each of said overshoots.

Claim 9 (original): The write current circuit of Claim 8, wherein said further circuit and said delay circuit are programmable for providing differential overshoot amplitudes and pulse widths for said positive write edge and said negative write edge.

Claim 10 (previously presented): A write driver for an inductive head element in a disk drive system, said driver comprising:

an H-bridge circuit capable of driving a first current and a second current through said head element;

a boost circuit coupled with said H-bridge and operable for delivering a current pulse during time periods defining a positive edge of said first current and a negative edge of said first current responsive to a control signal, wherein a sum of said first current and said second current provides the write current for said head element;

said boost circuit is further adapted to selectively vary said positive edge current pulse and said negative edge current pulse; and

a circuit coupled with the head write driver circuit and adapted to selectively provide pulsing signals which independently define an overshoot amplitude of said positive write edge and said negative write edge respectively of said write current signal.

Claim 11 (original): The write driver of Claim 10, wherein said boost circuit includes a programmable differential current source.

Claim 12 (original): The write driver of Claim 10, wherein said boost circuit is further adapted to selectively provide a defined amplitude for each of said positive edge current pulse and said negative edge current pulse.

Claim 13 (original): The write driver of Claim 12, wherein said boost circuit is programmable for providing differential amplitudes for said positive edge current pulse and said negative edge current pulse.

Claim 14 (original): The write driver of Claim 10, wherein said boost circuit further includes a delay circuit for selectively providing a defined pulse width for each of said positive edge current pulse and said negative edge current pulse.

Claim 15 (original): The write driver of Claim 14, wherein said delay circuit is programmable for providing differential pulse widths for said positive edge current pulse and said negative edge current pulse.

Claim 16 (original): The write driver of Claim 10, wherein said boost circuit is further adapted to selectively provide a defined amplitude for each of said positive edge current pulse and said negative edge current pulse and further includes a delay circuit for selectively providing a defined pulse width for each of said positive edge current pulse and said negative edge current pulse.

Claim 17 (original): The write driver of Claim 16, wherein said boost circuit and said delay circuit are programmable for providing differential amplitudes and pulse widths for said positive edge current pulse and said negative edge current pulse.

[redacted]

Claim 18 (original): A method of providing a write current to an inductive head element in a disk drive system, comprising:

providing current pulses cooperable for defining a positive edge and a negative edge of said write current;

differentially varying an amplitude of said positive edge current pulse and said negative edge current pulse for counteracting induced imbalances in said write current.

Claim 19 (original): The method of Claim 19 further comprising varying a pulse width of said positive edge current pulse and said negative edge current pulse for further counteracting induced imbalances corresponding to said disk drive system.

EVIDENCE APPENDIX

Appellants are submitting no items of evidence.

RELATED PROCEEDINGS APPENDIX

Appellants have no submission for the Related Proceeding Appendix.